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(54) Method for fabricating multi-level interconnection structure for semiconductor device.

(57) A method for fabricating a semiconductor device includes the steps of forming an interconnect metal film (33) on an insulating layer (32) and forming, on a surface of the interconnect metal film, a first insulating film (34) formed of P-SiN. The first insulating film (34) and the interconnect metal film (33) are simultaneously patterned to form a lower interconnect (33A). On the resulting surface, a second insulating film (35) having a polishing rate higher than that of the first insulating film (34) is formed. The entire surface of the second insulating film (35) is flattened by a chemical mechanical polishing process using the first insulating film (34) as a stopper. Then, on the resulting surface, a third insulating film (36) is formed. According to one embodiment, the first insulating film (34) used as the stopper remains on the lower interconnect (33A) but not between adjacent interconnects and, according to another embodiment, such film (34) is completely removed by etching. Thus, an increase in the capacitance between the interconnects is prevented and any stress migration therein is suppressed.

FIG. 3A

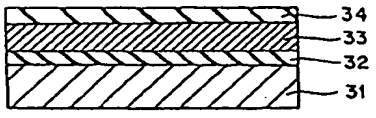


FIG. 3B

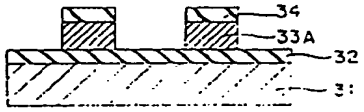


FIG. 3C

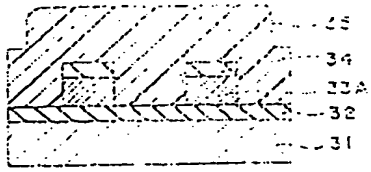


FIG. 3D

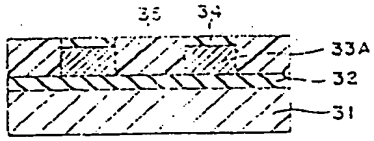
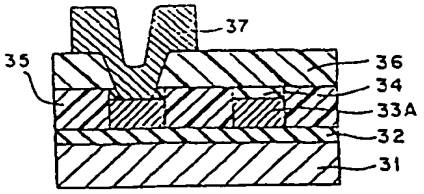


FIG. 3E



EP 0 602 607 A1

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The present invention relates to a method for fabricating a semiconductor device, and more particularly to a method for fabricating a semiconductor device in which an interlayer insulating film in a multi-level interconnection structure is flattened or planarized.

(2) Description of the Related Art

With an increased need for highly dense multi-level interconnections in a semiconductor device, there is a stronger requirement for an interlayer insulating film formed between metal interconnect layers to be perfectly flat and planar. In an attempt to meet such requirement, there has been proposed a method whereby a surface of the interlayer insulating film is polished by a Chemical Mechanical Polishing process (hereinafter referred to as "CMP process") which is a mechanical polishing process using a chemical agent. Figs. 1A through 1D are for showing an example of such process. Fig. 1A shows a state in which, after an aluminum interconnect layer 13 is formed in a predetermined pattern as a lower interconnect layer on a surface of an insulating film 12 on a semiconductor substrate 11, a plasma silicon oxide film (hereinafter referred to as "P-SiO film") 14 is formed as an interlayer insulating film. Then, the P-SiO film 14 is subjected to polishing of the CMP process and its surface is made flat as shown in Fig. 1B. Thereafter, though not shown in the drawings, an aluminum interconnect layer is formed as an upper interconnect layer and this completes the fabrication of a multi-level interconnect structure.

In a surface planarization technique using the CMP process, it is necessary that the polishing or lapping of the P-SiO film 14 be stopped at an exact timing when it has reached a certain predetermined thickness. However, it is difficult to know and determine the exact timing for stopping the polishing. If the amount of the polishing is excessive, the lower aluminum film 13 may be polished thereby reducing the thickness thereof as seen in Fig. 1C. On the contrary, if the amount of the polishing falls short, the P-SiO film 14 becomes too thick, as seen in Fig. 1D, in which case a step or uneven surface topography is not satisfactorily removed with a result that the surface planarization is insufficient.

In the conventional method described above, it has been the practice to determine the amount of polishing from the time converted and calculated from the polishing rate of the insulating film concerned. This involves a problem in that no appropriate polishing can be achieved when there is a change in the polishing rate itself.

As a way to solve the above problem, there has been proposed a surface planarization technique which utilizes an insulating film having a low polishing rate. That is, as shown in Fig. 2A, after an aluminum interconnect layer 23 is formed in a predetermined pattern as a lower interconnect on a surface of an insulating film 22 on a semiconductor substrate 21, a plasma silicon nitride film (hereinafter referred to as "P-SiN film") 24 as an interlayer insulating film having a low polishing rate is deposited to a thickness of about 0.3 μm by a Plasma-assisted Chemical Vapor Deposition (PCVD) on the overall surface of the device. Then, the P-SiO film 25 is deposited to a thickness of about 1.5 μm on the P-SiN film 24 by the PCVD process.

Thereafter, as shown in Fig. 2B, the overall surface of the resulting films is polished. The polishing rate of the P-SiN film 24 then is about 1/5 that of the P-SiO film 25 so that, when the polishing reaches a point where the P-SiN film 24 exposes its portion having a step therein, the overall polishing rate is lowered. For this reason, even when there is a slight error in the polishing time, it is possible to avoid the exposure and polishing of the aluminum interconnect layer 23 caused by the extended polishing time.

As shown in Fig. 2C, on the entire surface planarized as described above, a P-SiO film 26 is deposited to a thickness of about 0.8 μm to form an interlayer insulating film. Then, as shown in Fig. 2D, this interlayer insulating film 26 is provided with a through-hole and an upper aluminum pattern 27 is formed thereon and this completes the multi-level interconnect structure.

In the above described surface planarization technique, the P-SiN film 24 is utilized as a stopper when the P-SiO film 25 is polished by the CMP process. The use of the P-SiN film as a stopper in this way has been disclosed, for example, in Japanese Patent Application Kokai Publication No. Sho 62-216344 and Kokai Publication No. Sho 63-207153. However, the examples disclosed in these publications relate to the use of the P-SiN film as a stopper when a metal is polished.

Thus, conventionally, for making the interlayer insulating film flat, the P-SiN film has been used as a stopper in the CMP process. However, since the P-SiN film is formed in the entire surface area that includes the aluminum interconnects, the P-SiN film remains between adjacent interconnects after the completion of the multi-level interconnect structure. The dielectric constant of the P-SiN film is as large as about 8 so that line capacitance between the interconnects in the completed interconnect structure becomes large accordingly, and this possibly results in the deterioration of operation char-

acteristics, that is, the slowing of operation speeds in a semiconductor device.

Also, since the stress in the P-SiN film is large, the aluminum interconnects receive stresses in the course of, for example, a subsequent thermal process or accelerated test, and this leads to a problem of the so-called "stress migration" in which a void or a break is caused to occur in the aluminum interconnects.

SUMMARY OF THE INVENTION

It is, therefore, an object of the present invention to overcome the problems existing in the prior art and to provide an improved method for fabricating a semiconductor device in which an interlayer insulating film is planarized and which is constituted by a highly reliable multi-level interconnect structure.

It is another object of the invention to provide a method for fabricating a multi-level interconnect structure which is capable of suppressing an increase in the capacitance between interconnects and also an occurrence of stress migration therein.

According to one aspect of the invention, there is provided a method for fabricating a semiconductor device having a multi-level interconnection structure, the method comprising the steps of:

forming an insulating layer on a semiconductor substrate;

forming an interconnect metal film on the insulating layer;

forming, on an entire surface of the interconnect metal film, a first insulating film having a low polishing rate in a chemical mechanical polishing process;

sequentially and selectively etching the first insulating film and the interconnect metal film to form a lower interconnect;

forming, on an entire resulting surface, a second insulating film having a polishing rate higher than that of the first insulating film, so that the lower interconnect and the first insulating film which remains on the lower interconnect are completely buried in the second insulating film;

lapping down a surface of the second insulating film by the chemical mechanical polishing process using the first insulating film as a stopper thereby forming a planarized surface of the first and second insulating films; and

forming a third insulating film on the planarized surface of the first and second insulating films.

According to another aspect of the invention, the above method for fabricating the semiconductor device may further comprise a step for etching a surface of the first insulating film and a surfac of the second insulating film under a condition of etching rates common to both the surfaces, so that the first insulating film on the lower interconnect is removed.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will be apparent from the following description of preferred embodiments of the invention explained with reference to the accompanying drawings, in which:

Figs. 1A through 1D are diagrammatic sectional views for explaining the process steps in a conventional method for fabricating a semiconductor device using a CMP process;

Figs. 2A through 2D are diagrammatic sectional views for explaining the process steps in another conventional method for fabricating a semiconductor device using a CMP process;

Figs. 3A through 3E are diagrammatic sectional views for explaining the process steps in a method for fabricating a semiconductor device according to a first embodiment of the present invention; and

Figs. 4A through 4E are diagrammatic sectional views for explaining the process steps in a method for fabricating a semiconductor device according to a second embodiment of the present invention.

PREFERRED EMBODIMENTS OF THE INVENTION

Now, preferred embodiments of the invention are explained with reference to the accompanying drawings.

Figs. 3A through 3E show, in diagrammatic sectional views, a structure of a first embodiment according to the invention for explaining the process steps for fabricating the multi-level interconnection structure. As seen in Fig. 3A, an aluminum silicon copper alloy (Al Si Cu alloy) film 33 is deposited to a thickness of about 0.5 μm as a lower interconnect by a sputtering method on an insulating film 32 located on a surface of a semiconductor substrate 31. The lower interconnect may be formed by the CVD method in place of the sputtering method. Then, on the entire surface of the aluminum silicon copper alloy film 33, a P-SiN film 34 is deposited to a thickness of about 0.3 μm by, for example, the PCVD process. Thereafter, on the P-SiN film 34, a photoresist film (not shown) is applied and is developed into a pattern and, with this pattern used as a mask, the P-SiN film 34 and the lower interconnect layer 33 are sequentially and selectively etched by such a method as a selective ion-etching, whereby a lower interconnect 33A is formed in a desired pattern as shown in Fig. 3B.

Next, as shown in Fig. 3C, on the entire resultant surface, a P-SiO film 35 is grown to a thickness of 1.5 μm as an interlayer insulating film by, for example, the PCVD process, whereby the lower interconnect 33A and the P-SiN film 34 are completely buried therein. Then, by employing the CMP process, the P-SiO film 35 is polished until this film reaches a predetermined thickness. By this polishing, a surface of the P-SiO film 35 is made flat as seen in Fig. 3D. In this CMP polishing process, the polishing rate of the P-SiN film 34 is about 1/5 that of the P-SiO film 35 as already explained so that, when the polishing of the P-SiO film 35 progresses to a state wherein the P-SiN film 34 exposes itself, the P-SiN film 34 acts as a polishing stopper and the polishing rate is then reduced to 1/5 of the polishing rate theretofore.

For the above reason, in the polishing process to continue, even if a slight error is made in the polishing time, there will be no occurrence of a great error in the thicknesses of the P-SiN film 34 and the P-SiO film 35. That is, even when the polishing time is set somewhat longer, there will be no likelihood that the P-SiN film 34 is polished to such an extent that a surface of the lower interconnect 33A is also polished.

In this example, the desired polishing time is calculated based on the polishing rate obtained in advance and, by having the polishing progress controlled under such polishing time, the P-SiN film 34 is allowed to remain to a thickness of about 0.2 μm.

Thereafter, as seen in Fig. 3E, a P-SiO film 36 is deposited to a thickness in the order of 0.6 μm on the entire surface to form an interlayer insulating film. Needless to say that a surface of the interlayer insulating film 36 becomes flat because the surface the P-SiO film 35 is coplanar with the surface of the P-SiN film 34 by the CMP polishing. A through-hole is opened in the interlayer insulating film 36 and the P-SiN film 34, and an upper interconnect layer 37 of, for example, aluminum alloy is formed. This completes the formation of the multi-level interconnect structure.

Since the multi-level interconnect structure according to this embodiment utilizes the P-SiN film 34 as a stopper in the CMP polishing process, there is no possibility for the lower interconnect 33A to be polished or the uneven surface topograph of the interlayer insulating film 35 to remain even when the polishing time is less strictly controlled and, thus, it is possible to accomplish the planarization of the surface as desired. The P-SiN film 34 used as the stopper is allowed to remain on the lower interconnect 33A but does not remain between adjacent interconnects, that is, at the sidewall portion of the lower interconnect 33A. Thus, even when the dielectric constant of th P-SiN film 34 is larger than that of, for example, a P-SiO film 35, there will be no significant increase in the capacitance between the adjacent interconnects and hence no deterioration in operation speeds in the fabricated semiconductor device. Also, since there is little influence from the stress in the P-SiN film 34, the occurrence of any stress migration can be suppressed.

Figs. 4A through 4E are diagrammatic sectional views for explaining the process steps for fabricating a structure of a second embodiment according to the invention. As shown in Fig. 4A, an aluminum silicon copper alloy (Al Si Cu alloy) film 43 is deposited to a thickness of about 0.5 μm as a lower interconnect by the sputtering method or the CVD method on an insulating film 42 located on a surface of a semiconductor substrate 41. Then, on the entire surface of the aluminum silicon copper alloy film 43, a P-SiN film 43 is deposited to a thickness of about 0.3 μm by the PCVD process. Thereafter, by a photolithographic technique, the P-SiN film 44 and the lower interconnect film 43 are sequentially and selectively etched by such a method as a selective ion-etching, whereby a lower interconnect 43A is formed in a desired pattern as shown in Fig. 4B.

Next, on the entire surface, a P-SiO film 45 is grown to a thickness of 1.5 μm as an interlayer insulating film whereby the lower interconnect 43A and the P-SiN film 44 are completely buried therein. Then, by employing the CMP process, the P-SiO film 45 is polished until this film reaches a predetermined thickness. By this polishing, a surface of the P-SiO film 45 is made flat as seen in Fig. 4C. In this CMP polishing process, the polishing rate of the P-SiN film 44 is about 1/5 that of the P-SiO film 45 so that, by using the P-SiN film 44 as a polishing stopper and controlling the polishing based on the polishing time obtained in advance from the polishing rate, the P-SiN film 44 is left behind to a thickness of about 0.2 μm.

The process steps up to this point are the same as those in the method according to the first embodiment explained above.

Next, by employing a parallel-plate reactive-ion etching (RIE) system using, for example, CF_4 as an etching gas, the entire surface is etched until the P-SiN film 44 completely disappears. By appropriately setting the conditions such as the concentration and the flow rate of the etching gas and also the pressure in the system, the etching rate of the P-SiN 44 and that of the P-SiO 45 can be made substantially the same and, in this way, the P-SiN film 44 and the P-SiO film 45 as the interlayer insulating films are caused to be etched uniformly without leaving any undesirable topography or a step on the surfaces of those films. As a result, the P-SiN film 44 on the lower interconnect

43A is completely removed as seen in Fig. 4D. Needless to say that, even though the surface of the lower interconnect 43A made from aluminum alloy is then exposed, the same is not etched.

Thereafter, as seen in Fig. 4E, a P-SiO film 46 is deposited by, for example, the PCVD process, to a thickness in the order of 0.8 µm on the entire surface to complete the interlayer insulating film. The surface of the interlayer insulating film 46 becomes flat because the surfaces of the underlying P-SiO film 45 have been flattened by the CMP polishing process and the RIE etching. A throughhole is opened in the interlayer insulating film 46 and an upper interconnect 47 of, for example, aluminum alloy is formed. This completes the formation of the multi-level interconnect structure.

In the multi-level structure thus formed according to this second embodiment of the invention, the P-SiN 44 used as the stopper in the CMP polishing process does not remain at all in the structure, which means that any increase in the capacitance between the adjacent interconnects or any occurrence of stress migration that may be due to the dielectric constant of the P-SiN 44 can be completely and reliably prevented.

As explained above, according to the first embodiment of the invention, the interconnect metal film and the first insulating film used as a stopper in the CMP polishing process are simultaneously patterned to form the lower interconnect. Then, the interlayer insulating film as the second insulating film is formed and this film is polished and planarized by the CMP process. The first insulating film constituted by, for example, a P-SiN film, does not remain between adjacent interconnects. The advantages of the invention thereby include the prevention of an increase in the capacitance between the adjacent interconnects and the enhancement of the reliability of the semiconductor device by suppressing the lowering of operation speeds in the semiconductor device and the occurrence of stress migration in the interconnects.

Also, according to the second embodiment of the invention, since the first insulating film used as the stopper in the CMP process is completely removed by etching, the first insulating film constituted by, for example, P-SiN does not remain at all in the multi-level interconnect structure. This results in a further improvement against the lowering of operation speeds in the semiconductor device and the occurrence of stress migration in the interconnects.

While the invention has been described in its preferred embodiments, it is to be understood that the words which have been used are words of description rather than limitation and that changes within the purview of the appended claims may be made without departing from the true scope and spirit of the invention in its broader aspects.

Claims

1. A method for fabricating a semiconductor device having a multi-level interconnection structure, said method characterized by comprising the steps of:

   forming an insulating layer (32) on a semiconductor substrate (31);

   forming an interconnect metal film (33) on said insulating layer;

   forming, on an entire surface of said interconnect metal film, a first insulating film (34) having a low polishing rate in a chemical mechanical polishing process;

   sequentially and selectively etching said first insulating film (34) and said interconnect metal film (33) to form a lower interconnect (33A);

   forming, on an entire resulting surface, a second insulating film (35) having a polishing rate higher than that of said first insulating film (34), so that said lower interconnect (33A) and said first insulating film (34) which remains on said lower interconnect are completely buried in said second insulating film;

   lapping down a surface of said second insulating film (35) by the chemical mechanical polishing process using said first insulating film (34) as a stopper thereby forming a planarized surface of said first and second insulating films (34,35); and

   forming a third insulating film (36) on said planarized surface of said first and second insulating films.

2. A method for fabricating a semiconductor device according to claim 1, in which said interconnect metal film (33) is formed by a sputtering method.

3. A method for fabricating a semiconductor device according to claim 1, in which each of said first, second and third insulating films (34,35,36) is formed by a plasma-assisted chemical vapor deposition method.

4. A method for fabricating a semiconductor device according to claim 1, in which said lower interconnect (33A) is formed by a selective ion-etching method.

5. A method for fabricating a semiconductor device according to claim 1, in which said first insulating film (34) is formed of a plasma silicon oxide (P-SiO) film.

6. A method for fabricating a semiconductor device according to claim 1, in which said first insulating film (34) is deposited to a thickness of about 0.3 μm on said interconnect metal film (33).

7. A method for fabricating a semiconductor device according to claim 1, in which said second insulating film (35) is formed of a plasma silicon nitride (P-SiN) film.

8. A method for fabricating a semiconductor device according to claim 1, in which said second insulating film is deposited to a thickness of about 1.5 μm.

9. A method for fabricating a semiconductor device having a multi-level interconnection structure, said method characterized by comprising the steps of:

forming an insulating layer (42) on a semiconductor substrate (41);

forming an interconnect metal film (43) on an insulating layer;

forming, on an entire surface of said interconnect metal film, a first insulating film (44) having a low polishing rate in a chemical mechanical polishing process;

sequentially and selectively etching said first insulating film (44) and said interconnect metal film (43) to form a lower interconnect (43A);

forming, on an entire resulting surface, a second insulating film (45) having a polishing rate higher than that of said first insulating film (44) so that said lower interconnect (43A) and said first insulating film (44) which remains on said lower interconnect are completely buried in said second insulating film (45);

lapping down a surface of said second insulating film (45) by the chemical mechanical polishing process using said first insulating film (44) as a stopper thereby forming a planarized surface of said first and second insulating films (44,45);

etching a surface of said first insulating film (44) and a surface of said second insulating film (45) under a condition of etching rates common to both said surfaces so that said first insulating film (44) on said lower interconnect is removed; and

forming a third insulating film (46) on said planarized surface of said second insulating film (45) and said lower interconnect.

10. A method for fabricating a semiconductor device according to claim 9, in which said first insulating film (44) is removed completely by employing a parallel-plate reactive-ion etching (RIE) system using CF_4 as an etching gas.

11. A method for fabricating a semiconductor device according to claim 10, in which a concentration and a flow rate of said etching gas and a pressure in said parallel-plate reactive-ion etching (RIE) system are controlled so that an etching rate of said first insulating film (44) becomes substantially the same as that of said second insulating film (45).

12. A method for fabricating a semiconductor device according to claim 9, in which said interconnect metal film (43) is formed by a sputtering method.

13. A method for fabricating a semiconductor device according to claim 9, in which each of said first, second and third insulating films (44,45,46) is formed by a plasma-assisted chemical vapor deposition method.

14. A method for fabricating a semiconductor device according to claim 9, in which said lower interconnect (43A) is formed by a selective ion-etching method.

15. A method for fabricating a semiconductor device according to claim 9, in which said first insulating film (44) is formed of a plasma silicon oxide (P-SiO) film.

16. A method for fabricating a semiconductor device according to claim 9, in which said first insulating film (44) is deposited to a thickness of about 0.3 μm on said interconnect metal film (43).

17. A method for fabricating a semiconductor device according to claim 9, in which said second insulating film (45) is formed of a plasma silicon nitride (P-SiN) film.

18. A method for fabricating a semiconductor device according to claim 9, in which said second insulating film is deposited to a thickness of about 1.5 μm.

FIG. 1A
PRIOR ART

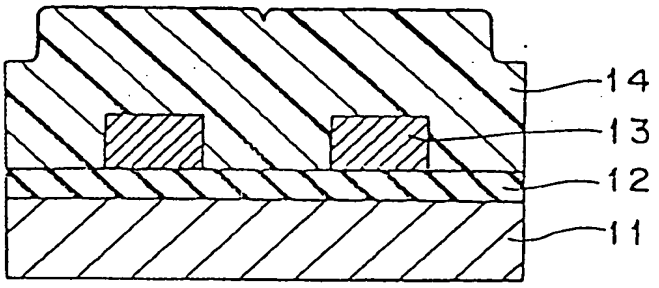


FIG. 1B
PRIOR ART

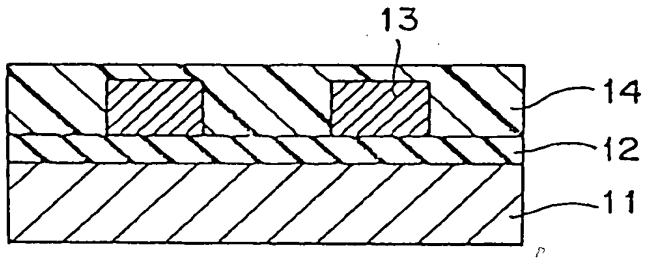


FIG. 1C
PRIOR ART

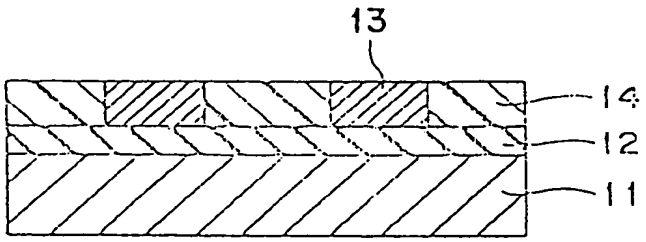


FIG. 1D
PRIOR ART

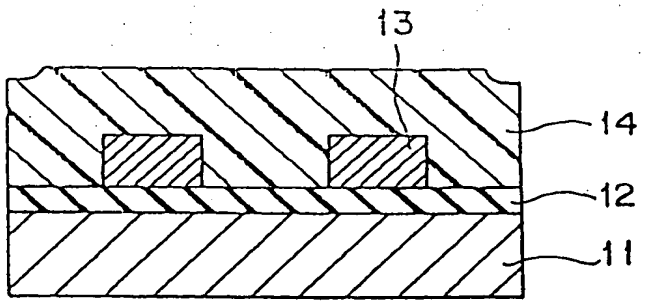


FIG. 2A
PRIOR ART

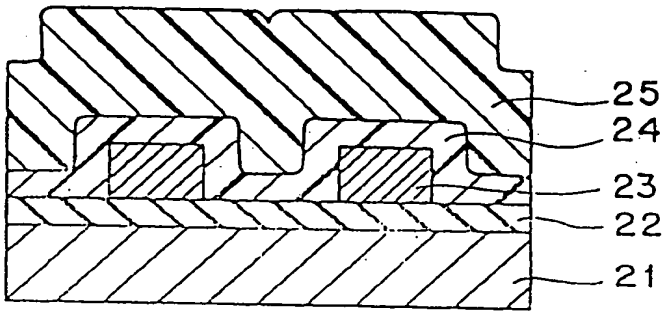


FIG. 2B
PRIOR ART

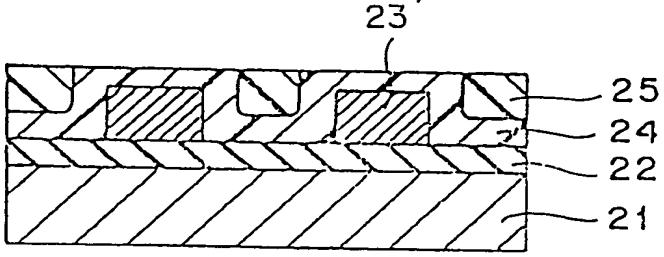


FIG. 2C
PRIOR ART

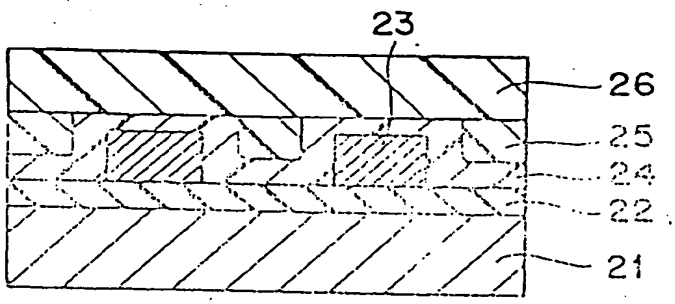


FIG. 2D
PRIOR ART

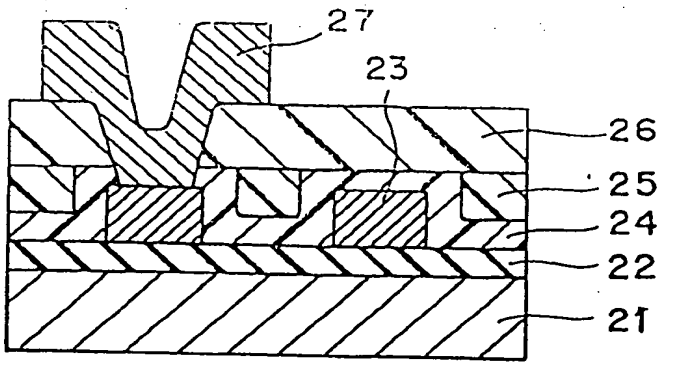


FIG. 3A

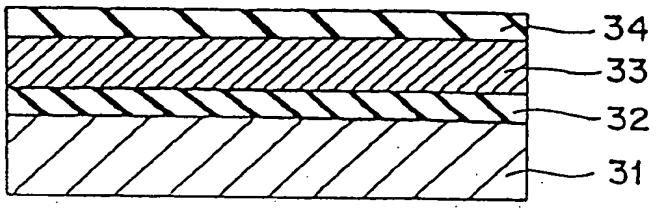


FIG. 3B

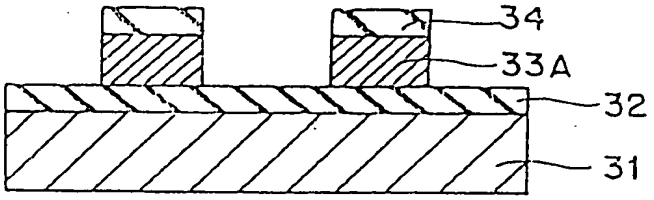


FIG. 3C

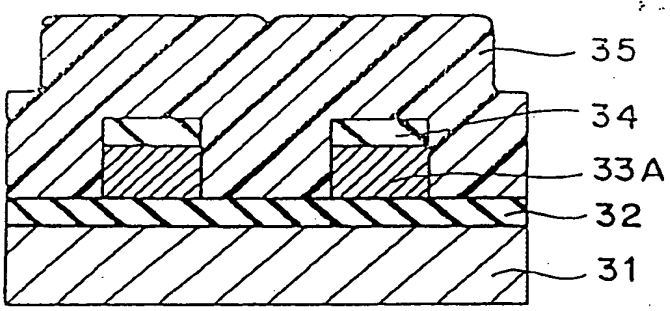


FIG. 3D

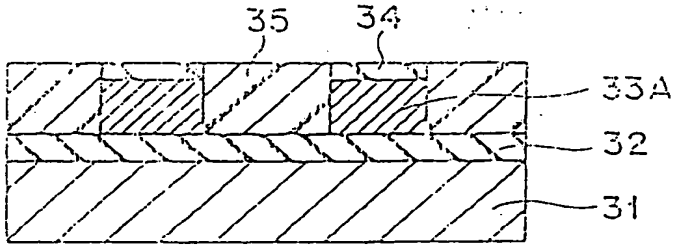


FIG. 3E

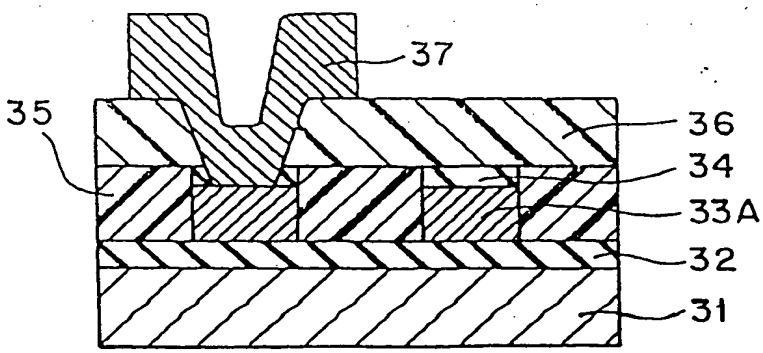


FIG. 4A

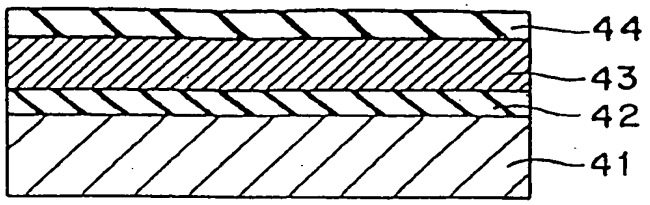


FIG. 4B

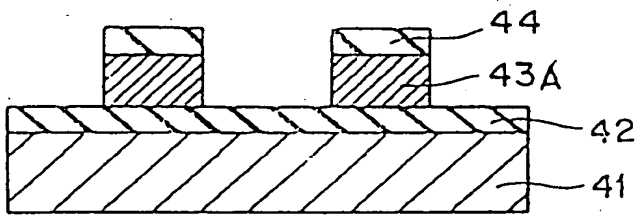


FIG. 4C

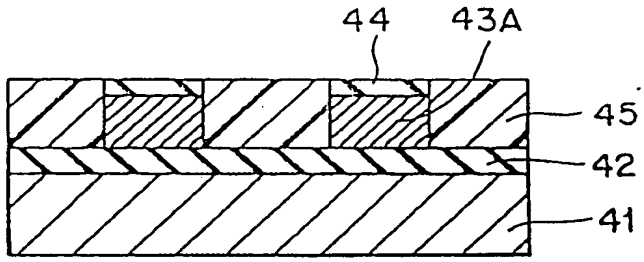


FIG. 4D

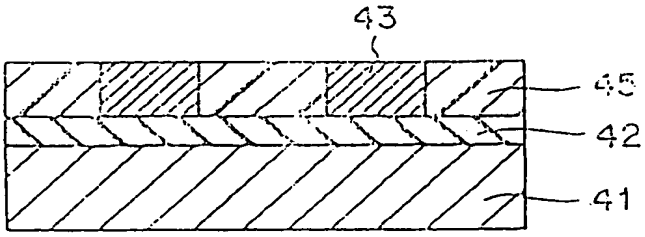


FIG. 4E